

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

Serial Number: 10/705,777

Filing Date: November 10, 2003

Title: SYSTEM AND METHOD FOR RACK MOUNT SYSTEM MID-PLANE INTERCONNECT USING SWITCHED TECHNOLOGY

Assignee: Intel Corporation

Page 8

Dkt: P9067D (INTEL)

REMARKS

As stated above, Applicant appreciates the Examiner's thorough examination of the subject application and request reexamination and reconsideration of the subject application in view of the preceding amendments and the following remarks. Applicant has carefully reviewed and considered the Office Action mailed on November 1, 2005, and the references cited therewith. Reconsideration and allowance of the subject application, as amended, are respectfully requested.

Claims 32, 37, 38, 41-44 and 47 have been amended, claims 33-36, 39, 40, 45 and 46 have been canceled; as a result, claims 32, 37, 38, 41-44 and 47 are now pending in this application.

Turning to substantive rejections, the Examiner rejects claims 32, 34, 35, 37-39 and 41-44, under 35 USC § 102(b) as being anticipated by Marshall et al. (U.S. Patent No. 4,605,915; hereinafter Marshall).

The Examiner points to Marshall as disclosing a parallel pair of copper conductors (11, 12) etched onto a surface of a lower half of an insulated laminate board, which in combination with an upper half of the laminated board encompasses the pair of copper conductors as described at column 2, line 64 to column 3, line 6. The Examiner points to Marshall as depicting in the alternate embodiment of Fig. 4, the encompassing laminate structure further includes upper vertical ground plane (115) disposed above the pair of copper conductors and lower vertical ground plane (116) disposed below the pair of copper conductors, and these ground planes are affixed to respective outer surfaces of the upper & lower half of the laminated boards. The Examiner points to Marshall as disclosing side ground planes (120) that are affixed to edges of the laminate board, such that one side ground plane is to the left of one of the copper conductors while the other side ground plane is to the right of the other side ground plane. The Examiner also notes that the side ground planes are oriented perpendicular to the vertical ground planes as well as being oriented parallel to the pair of copper conductors, as to provide an overall grounding shield for the copper conductors.

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

Serial Number: 10/705,777

Filing Date: November 10, 2003

Title: SYSTEM AND METHOD FOR RACK MOUNT SYSTEM MID-PLANE INTERCONNECT USING SWITCHED TECHNOLOGY

Assignee: Intel Corporation

Page 9

Dkt: P9067D (INTEL)

As mentioned above, independent claim 32 has been amended. In particular, the independent claim has been amended such that a pair of "side-ground-planes" and a pair of "vertical-ground-planes" are connected to form an open box structure that encompasses a pair of conductors. The claim has also been amended such that each of the side-ground-planes includes a pair of vias. Each pair of vias is used to connect the pair of vertical-ground-planes to one another (e.g., connect the top ground-plane to the bottom ground-plane). Marshall does not disclose or suggest a pair of "side-ground-planes" in which each includes a pair of vias for connecting a pair of "vertical-ground-planes".

In contrast, Marshall describes a stripline circuit that includes two coplanar striplines that are sandwiched within a dielectric material between an upper and a lower groundplane. In this regard Marshall states:

"The striplines and center groundplane are substantially coplanar. They are sandwiched within a dielectric material between two outer groundplanes. In the configuration illustrated in FIG. 1, the circuitboard is separated into two halves to show the striplines and center groundplane within. The upper half includes upper dielectric material 14a and the lower half includes lower dielectric material 14b. This dielectric material extends between outer groundplane 15 and outer groundplane 16 as illustrated." (col. 2, lines 54-63) (emphasis added)

However, Marshall is not understood to disclose or suggest a pair of vias in each one of a pair of side-ground-planes for connecting a pair of vertical-ground-planes. Rather, the reference describes that the upper and lower ground planes include holes for conductively interconnecting the upper and lower ground planes. In this regard Marshall states:

The two halves are bonded together using known means (such as a known dielectric adhesive) to form the completed circuitboard, and holes 17 are provided through the circuitboard at selected locations for use in conductively interconnecting the groundplanes with conductive connectors or plated-through holes. (col. 3, lines 7-12) (emphasis added)

Thus, Marshall is not understood to disclose or suggest a pair of vias in each one of a pair of side-ground-planes for connecting a pair of vertical-ground-planes. Since each and every limitation of Applicant's amended independent claim 32 is not disclosed or suggested in Marshall, Applicant respectfully submits that Marshall does not anticipate Applicant's invention

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

Serial Number: 10/705,777

Filing Date: November 10, 2003

Title: SYSTEM AND METHOD FOR RACK MOUNT SYSTEM MID-PLANES INTERCONNECT USING SWITCHED TECHNOLOGY

Assignee: Intel Corporation

Page 10
Dkt: P9067D (INTEL)

of amended independent claim 32. The remaining claims of this rejection depend directly or indirectly upon Applicant's invention of amended independent claim 32, and thus must be read as incorporating the limitations of the respective independent claims. (35 USC §112, 4th paragraph). Additionally, claims 32-36, 39, 40, 45 and 46 have been cancelled. Since nowhere does Marshall disclose or suggest these limitations of amended independent claim 32, it is respectfully submitted that the Examiner's rejection of claims 37, 38 and 41-44 as being anticipated by Marshall is in error, and should be withdrawn.

The Examiner also rejects claims 32-42 and 44, under 35 USC §103(a), as being unpatentable over Green et al. (U.S. Patent No. 2,034,034; hereinafter Green) in view of ordinary skill in the art.

The Examiner points to Green (Fig. 11) as disclosing a differential pair of parallel conductors (1, 2) which is encased by a dielectric casing or body (3). The Examiner also points to Green as disclosing a ground shield (3) that also surrounds the differential pair of conductors (1, 2). The Examiner notes that the ground shield comprises: side ground conductor portions which run parallel to the differential pair of conductors and which are respectively oriented to the left and the right of the differential pair of conductors (1, 2). The Examiner also notes that semi-circular vertical ground conductor portions which are respectively above and below the differential pair of conductors are connected to the side ground plane portions.

The Examiner concedes that Green differs from the claimed invention in that the material of the differential pair of conductors (1, 2) is not explicitly specified as being copper and that specific dimensional parameters of the differential pair of conductors is not explicitly disclosed. Based on ordinary skill in the art, the Examiner considers that it would have been obvious to have realized the differential pair of conductors as being formed of copper.

Similar to Marshall, Green does not disclose or suggest a pair of "side-ground-planes" that each includes a pair of vias for connecting a pair of "vertical-ground-planes", as required by amended independent claim 32.

In contrast, Green describes enclosing a pair of conductors in a conducting shield to reduce electromagnetic disturbances. In this regard Green states:

In accordance with the present invention it is proposed to enclose a pair of conductors in a conducting shield which acts to prevent external electromagnetic and electrostatic high-

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

Serial Number: 10/705,777

Filing Date: November 10, 2003

Title: SYSTEM AND METHOD FOR RACK MOUNT SYSTEM MID-PLANE INTERCONNECT USING SWITCHED TECHNOLOGY

Assignee: Intel Corporation

Page 11

Dkt: P9067D (INTEL)

frequency disturbances from causing disturbances in the circuit of the pair, and conversely to prevent currents transmitted over the pair from causing disturbances in external circuits. (col. 1, lines 22-30).

Thus, as understood by the Applicant, it appears that Green describes enclosing a pair of conductors and does not disclose or suggest a pair of "side-ground-planes" in which each includes a pair of vias for connecting a pair of "vertical-ground-planes".

For at least the reasons discussed above, Applicant respectfully asserts that amended independent claim 32 is patentable. Again, claims 32-36, 39, 40, 45 and 46 have been cancelled. As claims 37, 38, 41, 42 and 44 respectfully depend upon amended independent claim 32, Applicant respectfully asserts that claims 37, 38, 41, 42 and 44 are patentable over the combination of Green and ordinary skill in the art, and that the rejection should be withdrawn.

The Examiner also rejects claims 33, 36 and 40, under 35 USC §103(a), as being unpatentable over Marshall in view of ordinary skill in the art.

The Examiner points to Marshall as disclosing the claimed invention except for the specific dimensional parameters recited in the above identified claims. The Examiner appears to consider that the dimensional parameters would have been obvious within the purview of one of ordinary skill in the art.

As discussed above, Marshall is not understood to suggest or disclose suggest a pair of "side-ground-planes" in which each includes a pair of vias for connecting a pair of "vertical-ground-planes". Thus, Applicant asserts that independent claim 32 is patentable. Additionally, since claims 33, 36 and 40 have been cancelled; Applicant respectfully submits that the rejection should be withdrawn.

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (603-668-6560) to facilitate prosecution of this application.

Respectfully submitted,

ROBERT WACHEL

By his Representatives,

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

Serial Number: 10/705,777

Filing Date: November 10, 2003

Title: SYSTEM AND METHOD FOR RACK MOUNT SYSTEM MID-PLANE INTERCONNECT USING SWITCHED TECHNOLOGY

Assignee: Intel Corporation

Page 12
Dkt: P9067D (INTEL)**Customer Number: 45459**

603-668-6560

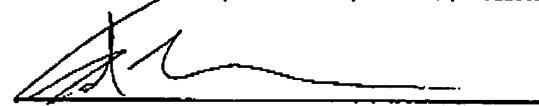
Date

2/1/06

By

Edmund P. Pfleger
Reg. No. 41,252**CERTIFICATE UNDER 37 CFR 1.8:** The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, P.O.Box 1450, Alexandria, VA 22313-1450, on this 1 day of February, 2006.Edmund Paul Pfleger

Name


Signature